Features

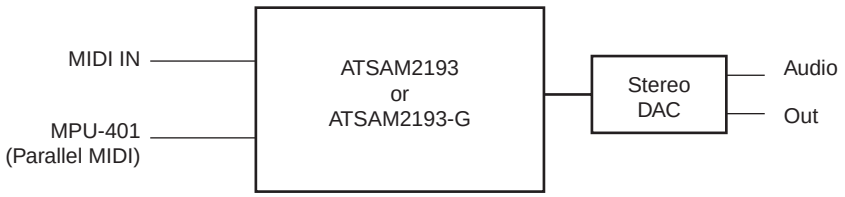
- **Single-chip All-in-one Design, Only Requires External DAC**
  - **MIDI Control Processor, Serial and Parallel Interface**
  - **Synthesis, General MIDI Wavetable Implementation**
  - **Compatible Effects: Reverb + Chorus**
  - **Spatial Effect**
  - **4-band Stereo Equalizer**
- **State-of-the-art Synthesis for Best Quality/Price Products**
  - **38-voice Polyphony + Effects**
  - **On-chip CleanWave™ Wavetable Data, Firmware, RAM Delay Lines**
- **Synthesizer Chipset: ATSAM2193/ATSAM2193-G + DAC**
- **Hardware Programmable DAC Mode**
  - **I2S: 16 to 20 bits**
  - **Japanese: 16 bits**
- **Typical Applications**
  - **Battery-operated Musical Keyboards**
  - **Portable Phones**
  - **Karaokes**
- **TQFP44 (10 mm x 10 mm) Package for ATSAM2193**
  TFBGA44 (7 mm x 7 mm) Package for ATSAM2193-G
  - **Both Options Provide Small Footprint, Low Pin Count**
- **Low-power**
  - **95 mW Typical Operating, <5 µA Power-down**
  - **2.5V and 3.3V Power Supply or Single 2.5V Supply**
  - **Built-in Power Switch**

Description

The ATSAM2193 provides a single-chip, low-cost MIDI sound system. Equipped with a serial and a parallel MIDI input, it provides state-of-the-art sound synthesis using a full GM sound set together with a range of compatible effects. Its low power consumption makes it ideal for all battery-powered applications such as portable Karaoke or any other device using MIDI synthesis.

The ATSAM2193-G has the same functionality as the ATSAM2193 but is presented in a TFBGA44 package.

Figure 1. Typical Hardware Configuration



Sound Synthesis

ATSAM2193 ATSAM2193-G Low-power Single-chip Synthesizer with Effects

Rev. 2695A–DRMSD–06/03

Pin Description

44-lead TQFP Package

Table 1. Pin by Function - 44-lead TQFP Package

Pin Name	Pin Number	Type	Function
Power Supply Group			
GND	9, 11, 20, 22, 30, 34, 38, 42	PWR	Digital ground - all pins should be connected to a ground plane.
VC3	10, 29	PWR	I/O power supply, 2.25V to 3.6V. All pins should be connected to a nominal 3.3V power.
VC2	1, 12, 32, 41, 44	PWR	Core power supply, 2.25V to 2.75V. All pins should be connected to nominal 2.5V. If the built-in power switch is used for minimum power-down consumption, then all these pins should be connected to the output of the power switch PWROUT (pin 36).
PWRIN	35	PWR	Power switch input, 2.25V to 2.95V. Even if the power switch feature is not used, this pin must be connected to nominal 2.5V.
Serial MIDI, Parallel MIDI (MPU-401)			
MIDI IN	17	IN	Serial TTL MIDI IN. Connected to the built-in synthesizer at power-up or after MPU reset. Connected to the D0 - D7 bus (read mode) when MPU switched to UART mode. This pin should be tied HIGH if not used.
D0 - D7	6, 8, 14, 16, 18, 21, 24, 26	I/O	8-bit bi-directional bus, under control of $\overline{CS}$, $\overline{RD}$, $\overline{WR}$. These pins should be left unconnected if not used.
A0	2	IN	This pin has built-in pull-down. Should be left unconnected if not used. Select: 0 = data registers (read/write) 1 = status register (read), control register (write)
$\overline{CS}$	4	IN	Chip select, active low. This pin has a built-in pull-down. It should be left unconnected if not used.
$\overline{RD}$	31	IN	Read, active low. When $\overline{CS}$ and $\overline{RD}$ are low, data (A0 = 0) or status (A0 = 1) is read on D0-D7. Read data is acknowledged on the rising edge of $\overline{RD}$. This pin has a built-in pull-down. It should be left unconnected if not used.
$\overline{WR}$	33	IN	Write, active low. When $\overline{CS}$ and $\overline{WR}$ are low, data (A0 = 0) or control (A0 = 1) is written from the D0 -D7 bus to the ATSAM2193 on the rising edge of $\overline{WR}$. This pin has a built-in pull-up. It should be left unconnected if not used.
IRQ	28	OUT	A rising edge indicates that a MIDI byte is available for read on D0 - D7. Acknowledged by reading the byte.
Digital Audio Group			
CLBD	3	OUT	Digital audio bit clock.
WSBD	23	OUT	Digital audio left/right select.
DABD	27	OUT	Digital audio stereo output.
DACSEL	15	IN	DAC type: 0 = I2S 16 to 20 bits 1 = Japanese 16 bits
Miscellaneous Group			
X1, X2	39, 40	-	9.6 MHz crystal connection. An external 9.6 MHz clock can also be used on X1 ($2.5V_{PP}$ max through 47 pF capacitor). X2 cannot be used to drive external circuits, use CKOUT instead.

Table 1. Pin by Function - 44-lead TQFP Package (Continued)

Pin Name	Pin Number	Type	Function
CKOUT	7	OUT	Buffered X2 output, can be used to drive external DAC master clock (256 * Fs)
LFT	43	-	PLL external RC network.
$\overline{\text{RESET}}$	5	IN	Reset input, active low. This is a Schmitt trigger input, allowing direct connection to an RC network.
PWROUT	36	PWR	Power switch output. Use this pin to supply 2.5V nominal core voltage by connecting it to all V_{C2} pins.
$\overline{\text{PDWN}}$	37	IN	Power down, active low. When power down is active, all outputs are set to logic level 0. The PLL and crystal oscillator are stopped. If the power switch feature is used, then 2.5V supply is removed from the core. To exit from power down, $\overline{\text{PDWN}}$ must be set to V_{C2}, then $\overline{\text{RESET}}$ applied. When unused this pin must be connected to V_{C2}.
TEST0 - TEST1	13, 25	IN	Test pins, should be grounded.
RUN	19	OUT	When high, indicates synthesizer is up and running.

Table 2. Pinout by Pin Number - 44-lead TQFP Package

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
1	VC2	12	VC2	23	WSBD	34	GND
2	A0	13	TEST0	24	D6	35	PWRIN
3	CLBD	14	D2	25	TEST1	36	PWROUT
4	$\overline{\text{CS}}$	15	DACSEL	26	D7	37	$\overline{\text{PDWN}}$
5	$\overline{\text{RESET}}$	16	D3	27	DABD	38	GND
6	D0	17	MIDI IN.	28	IRQ	39	X1
7	CKOUT	18	D4	29	VC3	40	X2
8	D1	19	RUN	30	GND	41	VC2
9	GND	20	GND	31	$\overline{\text{RD}}$	42	GND
10	VC3	21	D5	32	VC2	43	LFT
11	GND	22	GND	33	$\overline{\text{WR}}$	44	VC2

44-ball TFBGA Package

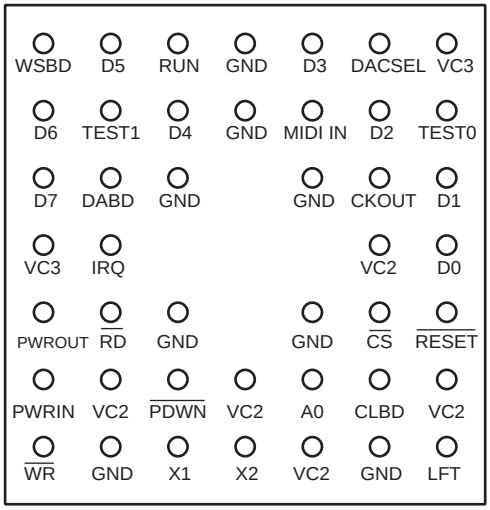
Table 3. Pin by Function - 44-ball TFBGA Package

Pin Name	Pin Number	Type	Function
Power Supply Group			
GND	A4, B4, C3, C5, E3, E5, G2, G6	PWR	Digital ground - all pins should be connected to a ground plane.
VC3	A7, D1	PWR	I/O power supply, 2.25V to 3.6V. All pins should be connected to a nominal 3.3V power.
VC2	D6, F2, F4, F7, G5	PWR	Core power supply, 2.25V to 2.75V. All pins should be connected to nominal 2.5V. If the built-in power switch is used for minimum power-down consumption, then all these pins should be connected to the output of the power switch PWROUT (pin 36).
PWRIN	F1	PWR	Power switch input, 2.25V to 2.95V. Even if the power switch feature is not used, this pin must be connected to nominal 2.5V.
Serial MIDI, Parallel MIDI (MPU-401)			
MIDI IN	B5	IN	Serial TTL MIDI IN. Connected to the built-in synthesizer at power-up or after MPU reset. Connected to the D0 - D7 bus (read mode) when MPU switched to UART mode. This pin should be tied HIGH if not used.
D0 - D7	D7, C7, B6, A5, B3, A2, B1, C1	I/O	8-bit bi-directional bus, under control of $\overline{CS}$, $\overline{RD}$, $\overline{WR}$. These pins should be left unconnected if not used.
A0	F5	IN	This pin has built-in pull-down. Should be left unconnected if not used. Select: 0 = data registers (read/write) 1 = status register (read), control register (write)
$\overline{CS}$	E6	IN	Chip select, active low. This pin has a built-in pull-down. It should be left unconnected if not used.
$\overline{RD}$	E2	IN	Read, active low. When $\overline{CS}$ and $\overline{RD}$ are low, data (A0 = 0) or status (A0 = 1) is read on D0-D7. Read data is acknowledged on the rising edge of $\overline{RD}$. This pin has a built-in pull-down. It should be left unconnected if not used.
$\overline{WR}$	G1	IN	Write, active low. When $\overline{CS}$ and $\overline{WR}$ are low, data (A0 = 0) or control (A0 = 1) is written from the D0 -D7 bus to the ATSAM2193 on the rising edge of $\overline{WR}$. This pin has a built-in pull-up. It should be left unconnected if not used.
IRQ	D2	OUT	A rising edge indicates that a MIDI byte is available for read on D0 - D7. Acknowledged by reading the byte.
Digital Audio Group			
CLBD	F6	OUT	Digital audio bit clock.
WSBD	A1	OUT	Digital audio left/right select.
DABD	C2	OUT	Digital audio stereo output.
DACSEL	A6	IN	DAC type: 0 = I2S 16 to 20 bits 1 = Japanese 16 bits
Miscellaneous Group			
X1, X2	G3, G4	-	9.6 MHz crystal connection. An external 9.6 MHz clock can also be used on X1 ($2.5V_{PP}$ max through 47 pF capacitor). X2 cannot be used to drive external circuits, use CKOUT instead.

Table 3. Pin by Function - 44-ball TFBGA Package (Continued)

Pin Name	Pin Number	Type	Function
CKOUT	C6	OUT	Buffered X2 output, can be used to drive external DAC master clock (256 * Fs)
LFT	G7	-	PLL external RC network.
$\overline{\text{RESET}}$	E7	IN	Reset input, active low. This is a Schmitt trigger input, allowing direct connection to an RC network.
PWROUT	E1	PWR	Power switch output. Use this pin to supply 2.5V nominal core voltage by connecting it to all V_{C2} pins.
$\overline{\text{PDWN}}$	F3	IN	Power down, active low. When power down is active, all outputs are set to logic level 0. The PLL and crystal oscillator are stopped. If the power switch feature is used, then 2.5V supply is removed from the core. To exit from power down, $\overline{\text{PDWN}}$ must be set to V_{C2}, then $\overline{\text{RESET}}$ applied. When unused this pin must be connected to V_{C2}.
TEST0 - TEST1	B7, B2	IN	Test pins, should be grounded.
RUN	A3	OUT	When high, indicates synthesizer is up and running.

Figure 2. Pinout by Pin Coordinate - 44-ball TFBGA (Top View)



Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Ambient Temperature (Power applied) ..... -40°C to +85°C Storage Temperature ..... -65°C to +150°C Voltage on Input Pins ..... -0.5V to V_{C3} + 0.3V (except X1 and $\overline{PDWN}$) Voltage on X1 and $\overline{PDWN}$ Pins ..... -0.5V to V_{C2} + 0.3V V_{C2} Supply Voltage (core) .....-0.5V to +3V V_{C3} Supply Voltage (I/O) .....-0.3V to +4.5V Maximum IOL per I/O pin ..... 4 mA	*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{C2}	Supply voltage	2.25	2.5	2.75	V
V_{C3}(1)	Supply voltage	2.5	3.3	3.6	V
t_A	Operating ambient temperature	0		70	°C

Note: 1. When using 3.3V VCC supply in a 5V environment, care must be taken that pin voltage does not exceed VC3+0.3V. Pin X1 is powered by VC2, therefore voltage on this pin should not exceed VC2+0.3V.
VC3 should not be lower than VC2.

DC Characteristics

Table 6. DC Characteristics (t_A = 25°C, V_{C2} = 2.5V ± 10%, V_{C3} = 3.3V ± 10%)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Low-level input voltage (Except X1, $\overline{PDWN}$)	-0.3	-	1.0	V
V_{IH}	High-level input voltage (Except X1, $\overline{PDWN}$)	2.3	-	V_{C3}+0.3	V
V_{IL}	Low-level input voltage for X1, $\overline{PDWN}$	-0.3	-	0.3	V
V_{IH}	High-level input voltage for X1, $\overline{PDWN}$	2	-	V_{C2}+0.3	V
V_{OL}	Low-level output voltage I_{OL} = -2mA	-	-	0.4	V
V_{OH}	High-level output voltage I_{OH} = 2mA	2.9	-	-	V
	Power consumption (crystal frequency =9.6 MHz)	-	95		mW
	Power down supply current (using power switch)		1	5	µA

Parallel MPU-401 Interface Timings

Figure 3. MPU Interface Read Cycle

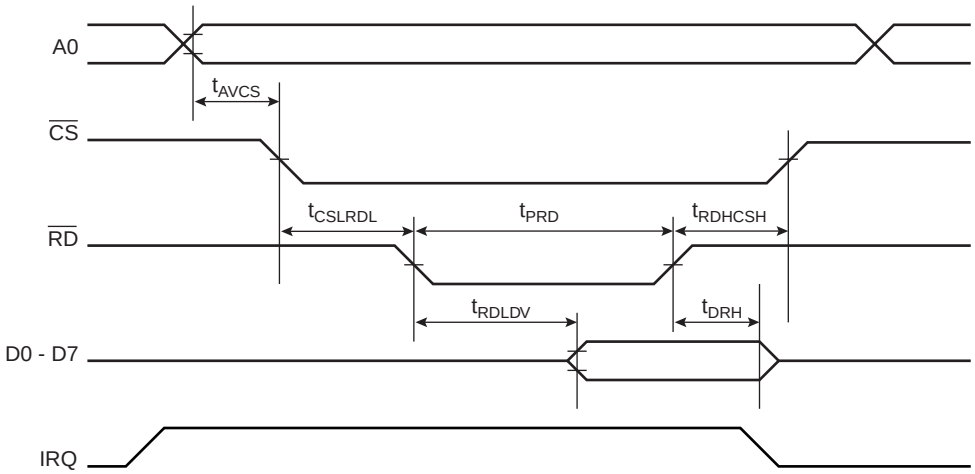


Figure 4. MPU Interface Write Cycle

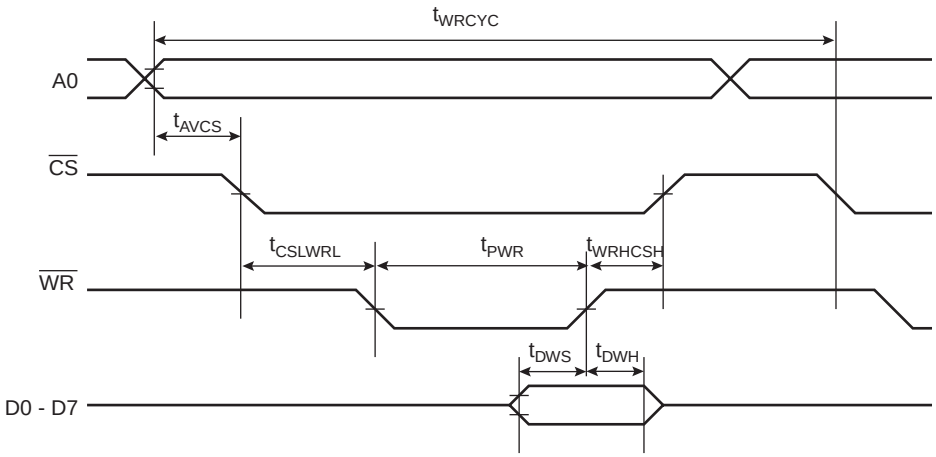


Table 7. MPU Interface Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{AVCS}	Address valid to chip select low	0	-	-	ns
t_{CSLRDL}	Chip select low to $\overline{RD}$ low	5	-	-	ns
t_{RDHCSH}	$\overline{RD}$ high to $\overline{CS}$ high	5	-	-	ns
t_{PRD}	$\overline{RD}$ pulse width	50	-	-	ns
t_{RDLDV}	Data out valid from $\overline{RD}$	-	-	20	ns
t_{DRH}	Data out hold from $\overline{RD}$	5	-	10	ns
$t_{CSLRWRL}$	Chip select low to $\overline{WR}$ low	5	-	-	ns
t_{WRHCSH}	$\overline{WR}$ high to $\overline{CS}$ high	5	-	-	ns
t_{PWR}	$\overline{WR}$ pulse width	50	-	-	ns
t_{DWS}	Write data setup time	10	-	-	ns
t_{DWH}	Write data hold time	0	-	-	ns
t_{WRCYC}	Write cycle	3	-	-	µs

Digital Audio Timings

Figure 5. Digital Audio

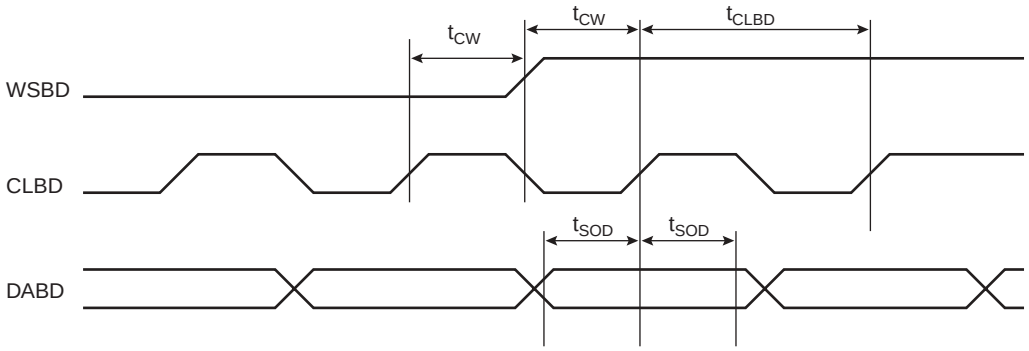
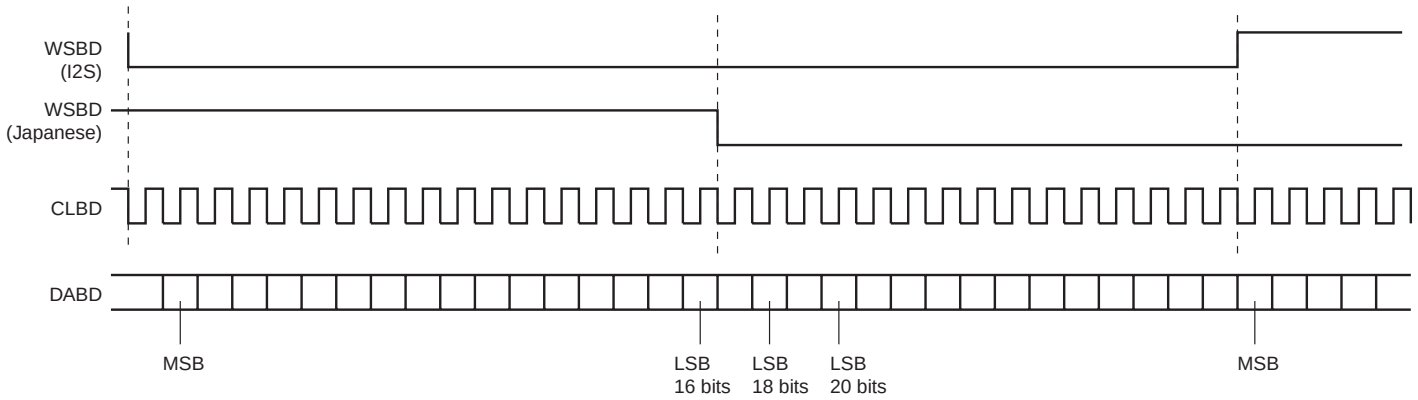


Table 8. Digital Audio Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{CW}	CLBD rising to WSBD change	200			ns
t_{SOD}	DABD valid prior/after CLBD rising	200			ns
t_{CLBD}	CLBD cycle time		416.67		ns

Figure 6. Digital Audio Frame Format



Notes: 1. Selection between I2S and Japanese format is via pin DACSEL.

Reset and Power-down

During power-up, the $\overline{\text{RESET}}$ input should be held low until the crystal oscillator and PLL are stabilized. This takes about 20 ms. A typical RC/diode power-up network can be used.

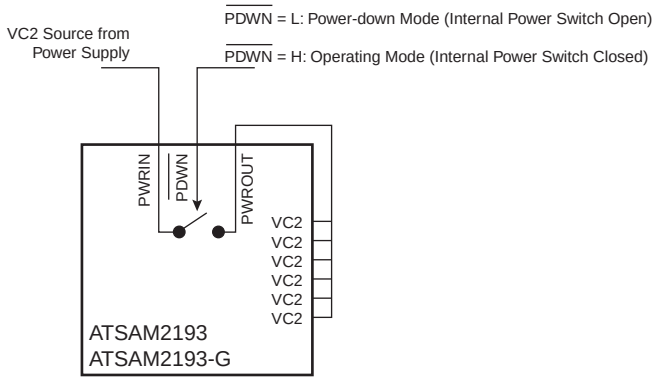
After $\overline{\text{RESET}}$, the ATSAM2193 or ATSAM2193-G enters an initialization routine. It takes around 50 ms before a MIDI IN or MPU message can be processed.

If $\overline{\text{PDWN}}$ is asserted low, then the crystal oscillator and PLL are stopped. The chip enters a deep power-down sleep mode. To exit power down, $\overline{\text{PDWN}}$ must be asserted high, then $\overline{\text{RESET}}$ applied.

Power-down mode is managed by an internal power switch. The equivalent schematic and standard connection is shown in Figure 7.

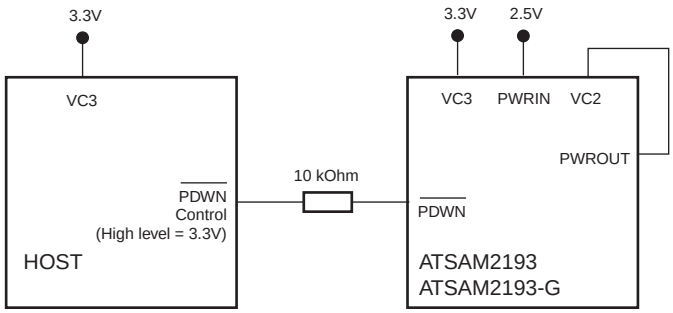
All the VC2 pins must be connected to PWROUT.

Figure 7. Schematic



Note: High level for $\overline{\text{PDWN}}$ is VC2 = 2.5V ±10%.

Figure 8. $\overline{\text{PDWN}}$ Connection Example



Recommended Board Layout

Like all HCMOS high integration ICs, the following simple rules of board layout are mandatory for reliable operation:

- GND, VC3, VC2 Distribution and Decouplings

All GND, VC3, VC2 pins should be connected. A GND plane is strongly recommended below the ATSAM2193 and ATSAM2193-G. The board GND + VC2 distribution should be in grid form.

Recommended VC2 decoupling is 0.1 µF at each corner of the IC with an additional 10 µF between pins 42 and 44 for the ATSAM2193 and between pins G6 and F7 for the ATSAM2193-G. VC3 requires a single 0.1 uF decoupling.

- Crystal, LFT

The paths between the crystal, the crystal compensation capacitors, the LFT filter R-C-R and the device should be short and shielded. The ground return from the compensation capacitors and LFT filter should be the GND plane from the device.

- Analog Section

A specific AGND ground plane should be provided, which is connected to the GND ground by a single trace. No digital signals should cross the AGND plane.

Refer to the Codec vendor recommended layout for correct implementation of the analog section.

Recommended Crystal Compensation and LFT Filter

Figure 9. ATSAM2193

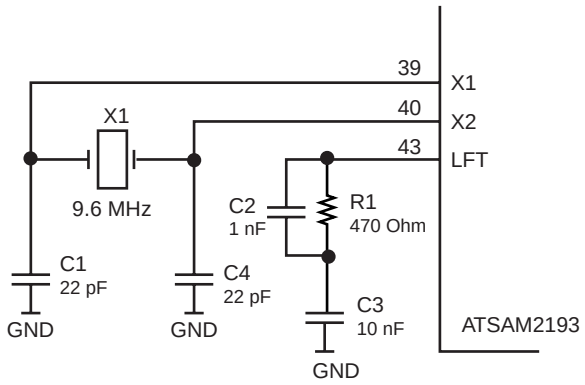
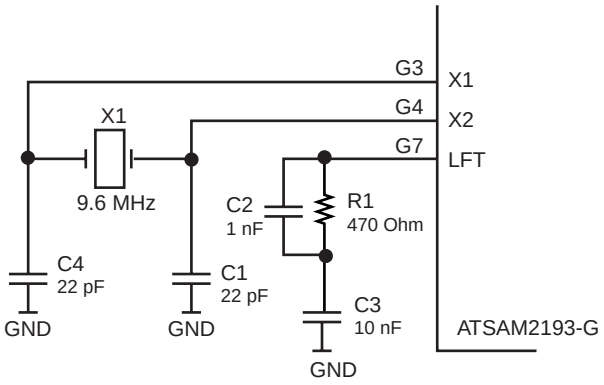


Figure 10. ATSAM2193-G



Mechanical Dimensions

44-lead TQFP Package

Figure 11. Thin Plastic 44-lead Quad Flat Pack (TQFP44)

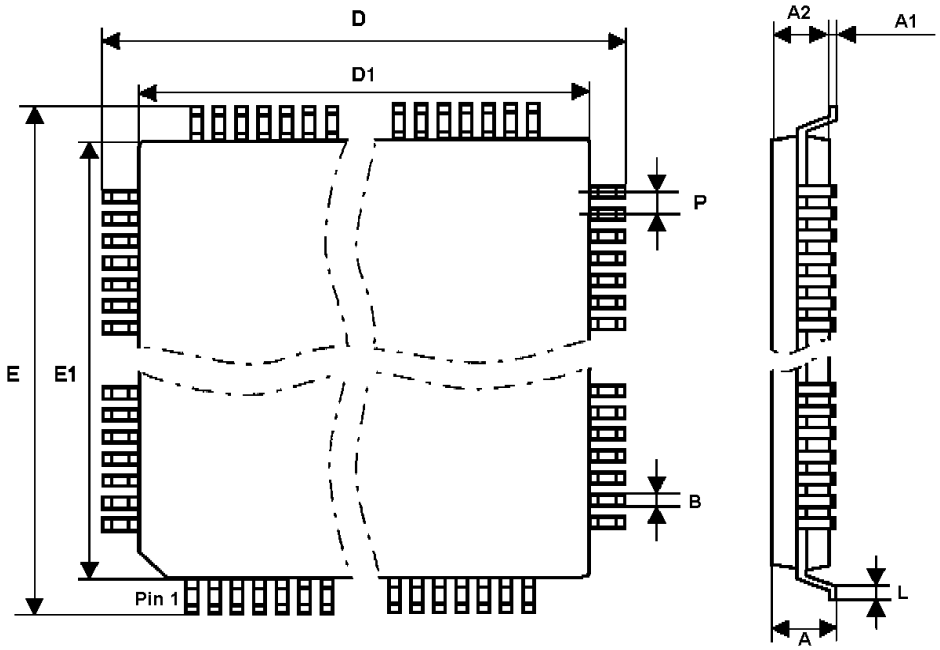


Table 9. 44-lead TQFP Package Dimensions (in mm)

Parameter	Min	Nom	Max
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
D		12.00	
D1		10.00	
E		12.00	
E1		10.00	
L	0.45	0.60	0.75
P		0.80	
B	0.3	0.37	0.45

44-ball TFBGA Package

Figure 12. 44-ball TFBGA Package

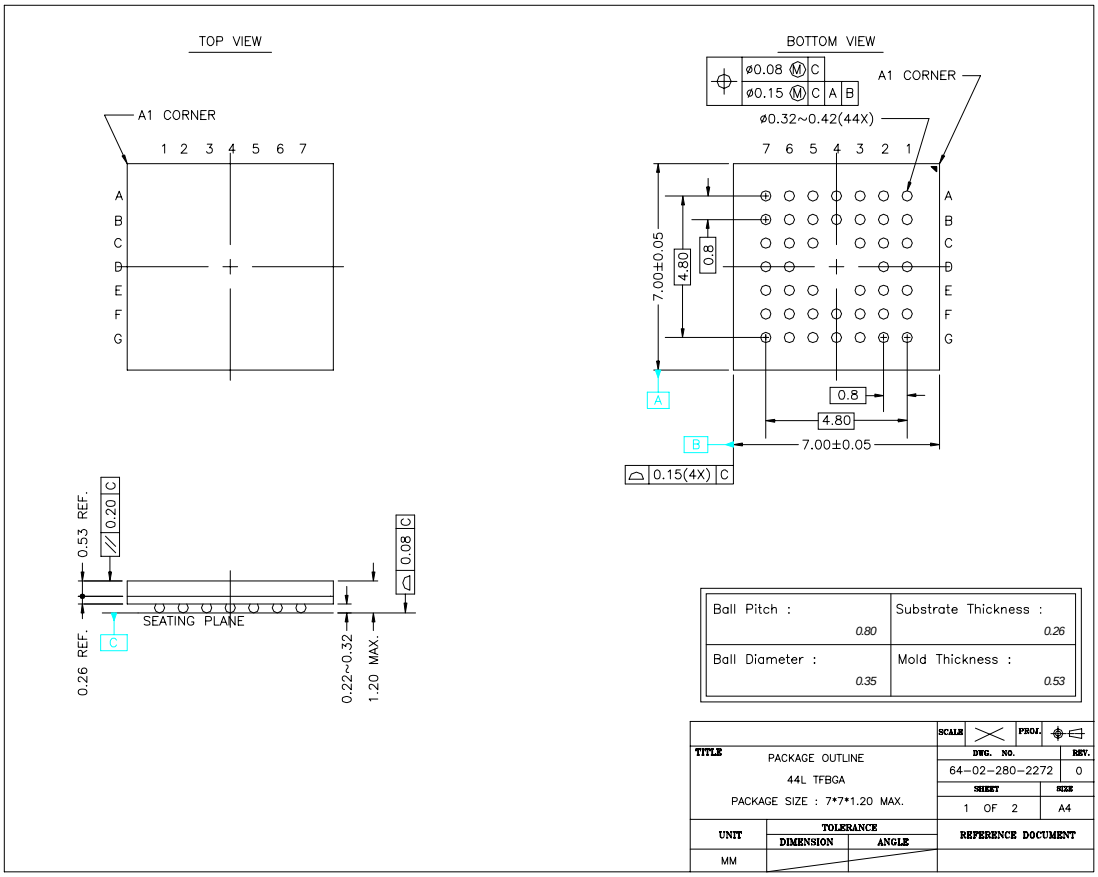


Figure 13. Package Marking

Note: A1 Ball in lower left-hand corner.

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